injected from the anode side are improved. Accordingly, the hole implantation from the anode side can be suppressed further in the built-in diode of the semiconductor device **4**.

[0089] Methods to further suppress the hole implantation from the anode side include methods that implant He or H^+ into the n^--type base layer **13** under the p-type base layer **16**. In the case where He or H^+ is implanted into the n^--type base layer **13**, the holes in the n^--type base layer **13** have shorter lives; and the hole implantation into the built-in diode is suppressed. However, such methods are problematic because the leak current during the reverse bias application increases at high temperatures and costs are high.

[0090] In the semiconductor device **4**, the implantation process of He or H^+ can be omitted; and a low-cost and highly-durable built-in diode is formed. The reverse recovery current is lower in the built-in diode even when switching from the forward bias to the reverse bias because the hole implantation from the anode side is suppressed by the n-type barrier layer **14**; and the response of the diode improves.

Fifth Embodiment

[0091] Modifications in which the trenches of the structures of FIG. **1** and FIG. **7** are shallower will now be described.

[0092] FIG. **11** is a schematic cross-sectional view of main components of a semiconductor device according to a fifth embodiment.

[0093] In the semiconductor device **5** illustrated in FIG. **11**, trenches **40**, **43**, **60**, and **63** are shallower than the trenches **20**, **23**, and **26** of the semiconductor device **1** and the trenches **30** and **33** of the semiconductor device **3**. A conductor layer **42** is formed inside the trench **40** with an insulating film **41** interposed. A conductor layer **45** is formed inside the trench **43** with an insulating film **44** interposed. A conductor layer **62** is formed inside the trench **60** with an insulating film **61** interposed. A conductor layer **65** is formed inside the trench **63** with an insulating film **64** interposed. The p-type base layer **16** is positioned between the trenches **40** and **43**; and the n^+-type emitter layer **17** contacts each of the trenches **40** and **43**. The conductor layers **62** and **65** are connected to the emitter electrode **81**.

[0094] For example, in the case where the trenches **20**, **23**, and **26** of the semiconductor device **1** illustrated in FIG. **1** are shallow, the apparent distance between the p-type diffusion layer **15** and the p-type base layer **16** shortens.

[0095] Then, a parasitic pnpn thyristor including the p-type base layer **16**, the n-type barrier layer **14**, the p-type diffusion layer **15**, and the n^--type base layer **13** operates easily; and there are cases where turn-off during operations at high current densities cannot be controlled and element breakdown occurs.

[0096] However, in the semiconductor device **5**, the distance from the p-type base layer **16** to the super junction of the n-type barrier layer **14** and the p-type diffusion layer **15** is lengthened by interposing the trenches **40** and **43** to avoid such a phenomenon; and the parasitic pnpn thyristor does not operate easily. Thereby, in the semiconductor device **5**, element breakdown due to turn-off defects can be avoided.

[0097] For the semiconductor device **3** illustrated in FIG. **7**, the potential of the conductor layers **42** and **45** which are gate electrodes is shielded from the p-type diffusion layer **15** by the conductor layers **62** and **65** which are emitter shield electrodes. Accordingly, the conductor layers **42** and **45** which are the gate electrodes are not easily affected by the potential fluctuations of the p-type diffusion layer **15**.

[0098] Here, the emitter-collector resistance can be reduced by p-type semiconductor layers **67** and **68** between the trench **40** and the trench **60** and between the trench **43** and the trench **63** having floating potentials. However, there is a risk of the gate capacitance (the gate-drain capacitance) increasing due to the potential fluctuation of the p-type semiconductor layers **67** and **68** which have floating potentials when switching. However, in the semiconductor device **5**, the volumes of the p-type semiconductor layers **67** and **68** are smaller than that of the p-type diffusion layer **15**. Accordingly, the gate capacitance can be reduced.

[0099] In the case where the p-type semiconductor layers **67** and **68** are connected to the emitter electrode **81** via a resistance element, the potential fluctuation of the p-type semiconductor layers **67** and **68** is suppressed and the gate capacitance is reduced. The emitter-collector resistance can be reduced further by reducing the volumes of the p-type semiconductor layers **67** and **68**.

[0100] The resistance recited above that connects the p-type semiconductor layers **67** and **68** to the emitter electrode **81** may be formed of polysilicon and may connect a portion of the p-type semiconductor layers **67** and **68** to the emitter electrode **81**.

Sixth Embodiment

[0101] FIG. **12** illustrates main components of an alternating current-direct current conversion circuit including an inverter circuit.

[0102] For example, as illustrated in FIG. **12**, an alternating voltage supplied from an alternating-current power source **75** is converted to a direct voltage by a converter **76**. A positive voltage is output from an output terminal **95** of the converter **76**; and a negative voltage is output from an output terminal **96**. The output terminals **95** and **96** are connected to an inverter **50**.

[0103] The inverter **50** is a three-phase inverter circuit having a so-called 6-in-1 structure (a structure in which six elements **51** to **56** are inside one circuit) and includes diodes **51***d* to **55***d* connected in anti-parallel to switching elements **51***t* to **56***t* respectively. The switching elements **51***t* to **56***t* are, for example, IGBTs; and the diodes **51***d* to **55***d* are, for example, FRDs (First Recovery Diodes).

[0104] The switching element **51***t* and the switching element **52***t* are connected in series; the switching element **53***t* and the switching element **54***t* are connected in series; and the switching element **55***t* and the switching element **56***t* are connected in series. The switching elements **51***t*, **53***t*, and **55***t* are connected to the output terminal **95**; and the switching elements **52***t*, **54***t*, and **56***t* are connected to the output terminal **96**. The intermediate point between the switching element **51***t* and the switching element **52***t* is connected to an output terminal **97**; the intermediate point between the switching element **53***t* and the switching element **54***t* is connected to an output terminal **98**; and the intermediate point between the switching element **55***t* and the switching element **56***t* is connected to an output terminal **99**. A three-phase alternating voltage is obtained from the output terminals **97**, **98**, and **99**.

[0105] By using the semiconductor device **2** described above, an inverter that uses individual IGBTs and FRDs (First Recovery Diodes) can be condensed into one semiconductor device **2**. Thereby, the circuit surface area and the cost are reduced. In particular, the response of the built-in diode improves in the case where the semiconductor device **2** is used. Accordingly, an inverter **50** having a good response is